

COMBINED DECLARATION
AND POWER OF ATTORNEY
FOR UTILITY OR DESIGN
PATENT APPLICATION

) Attorney Docket No.: 01-644
) 71742 (6653)
)
) First Named Inventor:
)
) Andreev, Alexander E.
)
) Application Number: TBD
)
) Filing Date: Herewith
)
) Group Art Unit: not yet assigned
)
) Examiner Name: not yet assigned

[X] Declaration [] Declaration
Submitted Submitted
With After
Initial Initial
Filing Filing

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

BUILT-IN TEST FOR MULTIPLE MEMORY CIRCUITS

the specification of which:

[X] is attached hereto, or

[] was filed by an authorized person on my behalf on _____ as United States Application Number _____ (Date)
or PCT International Application Number _____,
and was amended on _____ (if applicable).
(Date)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

Andreev et al.
Attorney Docket No. 01-725
71742 (6653)

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and I have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application, on this invention filed by me or my legal representatives or assigns and having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application Number(s)</u>	<u>Country</u>	<u>Foreign Filing Date</u>	<u>Priority Not Claimed</u>	<u>Certified Copy Attached</u>
				<u>Yes</u> <u>No</u>

N/A

[]Additional foreign application numbers are listed on a supplemental priority data sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

<u>Provisional Application Number(s)</u>	<u>Provisional Application Filing Date</u>
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N/A

[]Additional provisional application numbers are listed on a supplemental priority data sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code, §120, of any prior United States application(s), or under §365(c) of any PCT international application(s) designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information known by me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

<u>Prior U.S. Application Number</u>	<u>Prior PCT International Application Number</u>	<u>Filing Date of U.S. or PCT International Application</u>	<u>Patent Number (if applicable)</u>
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N/A

Andreev et al.
Attorney Docket No. 01-725
71742 (6653)

[] Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet attached hereto.

As a named inventor, I hereby appoint the following registered practitioners, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, and request that all correspondence and telephone calls in respect to this application be directed to:

LSI Logic Corporation
Corporate Legal Department
Intellectual Property Services Group
1551 McCarthy Blvd., M/S D-106
Milpitas, CA 95035
Telephone 408-433-8708; FAX 408-433-7770

and I hereby further appoint:

Sandeep Jaggi	43,331
Leo J. Peters	33,562
Timothy R. Croll	36,771
Pete R. Scott	33,279
John C. Chen	39,136

Whose address is: LSI LOGIC CORPORATION, 1551 McCarthy Blvd., Milpitas, CA 95035; Telephone No. (408) 433-8000

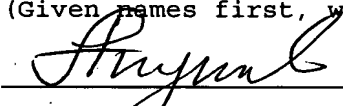
and I hereby further appoint:

<u>Registered Practitioner</u>	<u>Reg.No.</u>	<u>Registered Practitioner</u>	<u>Reg.No.</u>
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Julius Tabin	16,754	Bruce R. Mansfield	29,086
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Robert B. Jones	20,135	Karl R. Fink	34,161
James J. Schumann	20,856	Thomas F. Lebens	38,221
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Robert J. Fox	27,635	Charles W. Peterson, Jr.	34,406
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I hereby declare that all statements made herein of my own knowledge are true, and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity or enforceability of the application or any patent issued thereon.

Full name of sole or one joint inventor: Alexander E. Andreev
(Given names first, with Family name last)

Inventor's signature: 

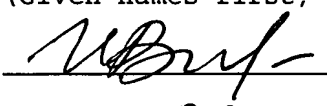
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Date:

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